IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. MA-068

In re patent application of
Maitreyee Mahajani et al.

Serial No. 10/079,472 Group Art Unit: 2814

Filed: February 19, 2002 Examiner: Thao X. Le

For: GATE DIELECTRIC STRUCTURES FOR INTEGRATED CIRCUITS AND METHODS FOR MAKING AND USING SUCH GATE DIELECTRIC STRUCTURES

REPLACEMENT BRIEF ON APPEAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

November 22, 2005

To the Commissioner:

This replacement Brief on Appeal is filed in response to a Notification of Non-Compliant Appeal Brief mailed October 28, 2005. Appellants hereby appeal the April 20, 2005 final rejection of claims 9, 12-15, 24, 26, and 36-38 in the above-identified application to the Board of Patent Appeals and Interferences.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date below.

Pamela J. Squyres, reg. no. 52,246

11/23/05
Date of Deposit

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest is Matrix Semiconductor, Inc., a Delaware corporation.

II. RELATED APPEALS AND INTERFERENCES

The undersigned is not aware of other related appeals and interferences.

III. STATUS OF CLAIMS

Claims 3, 5-9, 12-15, 23-26, 28-29, 32-33, 36-38, and 40-42 are pending in the application. Claims 3, 5-8, 23, 25, 28, 29, 32, 33, and 40-42 have been withdrawn from consideration by the Examiner over the objections of Appellants. Claims 9, 12-15, 24, 26, and 36-38 have been finally rejected and are the subject of this appeal. A listing of the appealed claims is presented in the APPENDIX.

IV. STATUS OF AMENDMENTS

No amendments after final rejection were filed.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A SONOS device is a field effect transistor that operates as a nonvolatile memory cell by storing charge. A conventional SONOS device (shown in Fig. 1 of the present application) consists of a monocrystalline silicon substrate 15, a tunneling oxide layer 25 formed on the substrate, a silicon nitride charge storage layer 35 formed on the tunneling oxide layer, a blocking oxide layer 30 formed on the silicon nitride layer, and a gate electrode 40 formed on the blocking oxide. The tunneling oxide 25 and blocking oxide 30 are conventionally formed of silicon dioxide, and the gate electrode 40 is conventionally polycrystalline silicon, known as *polysilicon*. The silicon-oxide-nitride-oxide-silicon stack of the silicon substrate, tunneling oxide, nitride, blocking oxide and polysilicon gate electrode give the SONOS device its name.

To program a SONOS memory cell, a charge is applied to the gate electrode. A channel region forms in the silicon substrate, and charge carriers, for example electrons, are attracted from the silicon substrate toward the gate electrode. (A charge carrier may be either an electron or a hole, which is a missing electron. For simplicity, this discussion will speak of migration of electrons.) Electrons tunnel through the tunneling oxide (toward the gate electrode) and are trapped in the nitride layer. When charge is removed from the gate electrode, electrons remain trapped in the nitride layer. The tunneling oxide prevents the trapped electrons from migrating back to the silicon channel region in the substrate, and the blocking oxide prevents electrons from migrating to the polysilicon gate electrode.

This stored charge changes the threshold voltage for the transistor, which is the applied gate voltage at which a transistor turns "on" or begins conducting, and thus can be detected. In this way, the SONOS device can store a memory state and behave as a memory cell. For example, a SONOS memory cell having stored charge can represent a data "1",

while a memory cell having no stored charge represents a data "0". The stored charge can be repeatedly removed from and returned to the nitride layer of a SONOS memory cell; in this way the cell can be erased and reprogrammed.

A more common type of transistor-based memory cell is a *floating gate* memory cell. In a floating gate memory cell, charge is stored in an electrically isolated, or "floating" polysilicon layer sandwiched between a tunneling oxide layer and a blocking oxide layer. The distinction between a SONOS memory cell and a floating gate memory cell is that the floating gate memory cell stores charge in a conductive material (a polysilicon floating gate) while the SONOS memory cell stores charge in a dielectric material (a silicon nitride layer.) The stored electrons are free to migrate within a floating gate, while they remains largely stationary within the nitride layer of a SONOS cell. This means that a single pinhole defect in, for example, the tunneling oxide of a floating gate memory cell can allow all of the stored charge in the floating gate to escape; because the charge cannot migrate freely within the nitride layer, SONOS cells are less susceptible to loss of stored charge through this mechanism.

The thickness and quality of the tunneling oxide is very important to the performance of a SONOS device. This layer must be thin enough to allow electrons to tunnel across it when the cell is being programmed, but must have very few defects to prevent loss of stored charge the rest of the time, when that charge is to be retained. Many methods can be used to form the tunneling oxide, including deposition of an oxide or thermal oxidation of the silicon substrate. In the present invention, a SONOS memory cell is taught in which the tunneling oxide is formed by a process of *in situ steam generation*, or ISSG. Through this method a very thin, very high-quality oxide layer can be made.

As noted, in a conventional SONOS transistor (as in most semiconductor transistors), the channel region is formed in a substrate, which is normally a monocrystalline silicon wafer. The wafer is essentially a single crystal of silicon. For most applications, the use of monocrystalline silicon is desirable. When a layer of silicon is deposited, it is typically polycrystalline, having many crystals and thus having grain boundaries, the boundaries between adjacent silicon grains in polycrystalline silicon. Grain boundaries impede current flow, making for slower devices.

A SONOS device may be formed having its channel region formed in a deposited polysilicon layer rather than in a monocrystalline silicon wafer substrate. A transistor formed having its channel region in a thin film of deposited polysilicon, rather than in a monocrystalline wafer substrate, is called a *thin film transistor* (TFT). A SONOS memory cell formed as a TFT will function as a memory cell, but will be a lower-speed, lower-performance device than a comparable device formed in monocrystalline silicon, with larger variations in performance between cells in the same memory array. Programming and read margins are smaller; thus in a TFT memory array of SONOS devices, use of an ISSG tunneling oxide to improve tunneling and charge retention is particularly advantageous.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

There are two grounds of rejection to be reviewed in this appeal:

1) Whether claims 9, 12-15, and 24 are anticipated by Halliyal et al., US Patent No. 6,674,138 ("Halliyal et al.", under 35 USC 102(e).

2) Whether claims 26 and 36-38 are anticipated by Halliyal et al. under 35 USC 102(e).

VII. ARGUMENT

A. Claims 9, 12-15, and 24 Are Not Anticipated by Halliyal et al.

Claim 9 recites a method for making a SONOS device, comprising providing a channel region; providing a first oxide layer on the channel region by an in-situ steam generation process; providing a silicon nitride layer on the first oxide layer; and providing a second oxide layer on the silicon nitride layer, wherein the device is a SONOS device.

The construction of the cell is very clearly defined in the claim: The first oxide layer is formed by ISSG on the channel region, the silicon nitride layer is formed on the first oxide layer, and the second oxide layer is formed on the silicon nitride layer. Each layer is formed on the one before it, so this is a contiguous stack, with no other layers intervening.

The Examiner points to the channel region 18, oxide layer 28, what he identifies as nitride layer 30, and oxide layer 32 of Fig. 1 of Halliyal et al. Layer 18 apparently corresponds to the channel region of claim 9, while oxide layer 28 and oxide layer 32 correspond to the first and second oxide layers of the claim. The disclosure of Halliyal et al., however, is clear that layer 30 cannot be characterized as a silicon nitride layer.

At col. 12, lines 1-33, Halliyal et al. describe various embodiments, including those in which layer 30 "comprises both a high-K dielectric material and a standard-K dielectric material" (lines 7-8); in which layer 30 "comprises a composite or a reaction product of two or more dielectric materials, at least one of which is a high-K dielectric material" (lines 9-12). In another embodiment, "high-K dielectric material completely replaces the nitride layer of a conventional ONO structure," (lines 16-17); in another "the high-K dielectric material is, in essence, added to or combined with, the nitride layer of a conventional ONO structure" (lines 17-19); in still another, "the layer includes a composite dielectric material which replaces the nitride layer of a conventional ONO structure" (lines 19-21).

Halliyal et al. explicitly define the term "high-K dielectric material" to mean "a dielectric material having a K of about 20 or more" (col. 5, lines 58-59.) As silicon nitride has a K between 6 and 9 (see col. 5, lines 47-48 and Table 1) it is specifically excluded, and is not considered to be a "high-K dielectric material."

One skilled in the art will expect a layer described as a "silicon nitride layer" to be formed of silicon nitride, perhaps including low levels of typical contaminants that might be expected to occur in a normal fabrication environment. One skilled in the art will not expect a layer described as a "silicon nitride layer" to include a high-K dielectric component sufficient to significantly change its function. In some embodiments of Halliyal et al., layer 30 includes *only* high-K dielectric material, and no silicon nitride, while *every* embodiment of Halliyal et al. includes *some* high-K dielectric layer or component. Simply put, layer 30 of Halliyal et al. cannot reasonably be described as a silicon nitride layer.

In the Response to Arguments (page 5) of the final rejection of April 20, the Examiner argues:

> Halliyal attempted to modify the ONO structure by using the high-K dielectric material in combination with silicon nitride layer 30 in various embodiments as described in column 12 lines 15-22. Thus, layer 30 would comprise silicon nitride and would read on the claim limitation. It has been held that the use of the term 'comprising' leaves a claim open for inclusion of material or steps other than recited in the claim ...

Appellants understand the Examiner to be saying that because claim 9 recites that the cell "comprises" silicon nitride, other materials may also be included between the tunneling oxide and blocking oxide.

Appellants, however, must disagree. Claim 9 does not recite a SONOS memory cell which *comprises* silicon nitride between the tunneling oxide and the blocking oxide. The claim recites a cell comprising a channel region and an oxide-silicon nitride-oxide stack, the channel region and stack being contiguous with no intervening elements. The word

"comprising" is indeed used in the claim, allowing for other unnamed elements in the memory cell (a gate electrode, source and drain regions adjacent to the channel, or wiring layers, for example) in addition to this channel region and stack, but not within or between them.

Independent claim 24 has similar language, and distinguishes over Halliyal et al. by the same rationale. Accordingly, Appellants respectfully request that the 35 USC 102(e) rejections of independent claim 9, its dependents 12-15, and independent claim 24 be withdrawn.

B. Claims 26 and 36-38 Are Not Anticipated by Halliyal et al.

Claim 26 recites an integrated circuit containing a SONOS semiconductor device made by a method comprising: providing a **polysilicon** layer; providing a first oxide layer on the polysilicon layer by an in-situ steam generation process; providing a silicon nitride layer on the first oxide layer; and providing a second oxide layer on the silicon nitride layer wherein the device is a SONOS semiconductor device. Claim 38 has similar language, while claims 36 and 37 add the limitation that the polysilicon layer is in fact a polysilicon *channel region*.

To summarize, independent claims 36 and 37 both include the limitation that a contiguous oxide-silicon nitride-oxide stack (the first oxide layer formed by ISSG) is formed on a *polysilicon channel region*, while independent claims 26 and 38 recite that this stack is formed on polysilicon or a polysilicon layer. The device is a TFT device. In all of these claims, the layers are formed in a SONOS device.

In rejecting claim 26 (near the bottom of page 3 of the final rejection), the Examiner says:

> Halliyal discloses an integrated circuit containing a SONOS semiconductor device made by the method comprising: providing polysilicon 16, column 10, line 3 ...

The passage the Examiner cites refers to Fig. 3, in which the substrate, labeled "16 or 44," referring to either monocrystalline silicon substrate 16 of Fig. 1 or polysilicon floating gate 44 of Fig. 2.

Halliyal et al. teach two separate embodiments, each using the dielectric stack including a high-K dielectric material which is not silicon nitride. The first embodiment, discussed in Section A, is shown in Fig. 1, and is a SONOS device having its channel region formed in a monocrystalline silicon substrate 16. Since the channel region is formed in monocrystalline silicon, it is not a TFT device.

It was described in the summary of the invention that an alternate type of memory cell, which is not a SONOS memory cell, is a floating gate memory cell. It will be recalled that a floating gate memory cell, like a SONOS memory cell, operates by storing charge. In contrast to a SONOS memory cell, however, in a floating gate memory cell, charge is stored in a polysilicon floating gate rather than in a silicon nitride layer.

Examples of SONOS and floating gate devices are shown in the Evidence Appendix, which includes Exhibits A and B.

Exhibit A is Bu et al, "Design Considerations in Scaled SONOS Nonvolatile Memory Devices". Fig. 1 of this paper contrasts the conventional floating gate and SONOS structures. The first paragraph of the Introduction includes the following sentence: "Two basic types of EEPROMs exist, namely, the floating gate device and the floating trap device, i.e. SONOS [3-4]." **Exhibit B** is an excerpt from Volume 28 of *Cx-News*, a semiconductor technical information online publication from Sony Electronics (http://www.sony.net/Products/SC-HP/cx_news/vol28/pdf/monos.pdf). In the second paragraph, this article gives an example of the terms "SONOS", "MONOS" and "floating gate" as used in the art:

> Figure 1 compares the MONOS and floating gate device structures. As can be seen in Figure 1, the MONOS name comes directly from the structure of the device. (In the US, silicon is used instead of metal, and it is called SONOS.) In MONOS, charge is stored in traps in the nitride layer, which is an insulator sandwiched between oxide layers, and this stored charge is used to record data.

It will be recalled that the layers of a conventional SONOS cell are, from the bottom up: a silicon channel region, a tunneling oxide, a *silicon nitride layer* to store charge, a blocking oxide, and a polysilicon gate electrode. In contrast, the layers of a conventional floating gate cell are, from the bottom up: a silicon channel region, a tunneling oxide, a *polysilicon floating gate* to store charge, a blocking oxide, and a polysilicon gate electrode.

The second embodiment of Halliyal et al., shown in Fig. 2 of that patent, is a floating gate memory cell, not a SONOS memory cell (col. 8, lines 66-67). As described in col. 8, line 66 through col. 9, line 6, it has the conventional channel region 18 (formed in monocrystalline silicon substrate 16), tunneling oxide 42, and floating gate 44. The stored charge 34 (indicated as "xxx" in Fig. 2) is stored in this floating gate 44 (col. 9, lines 10-12.) In a conventional floating gate memory cell, the next layer, above floating gate 44, would be a blocking oxide to prevent migration of charge from floating gate 44 to gate electrode 46.

Instead, Halliyal et al. have replaced the conventional blocking oxide with what they refer to as a "modified ONO stack", which consists of bottom oxide layer 28, a layer 30 including high-K dielectric, and top oxide layer 32. In the SONOS memory cell of Fig. 1, layer 28 served as a tunneling dielectric, layer 30 as a charge storage dielectric, and layer 32 as a blocking dielectric. In Fig. 1, stored charge 34a and 34b, indicated as "xxx" is shown stored in high-K dielectric layer 30.

In the embodiment of Fig. 2, however, layers 28, 30, and 32, which are together referred to as dielectric stack 26, play a different role. Layer 30 does not store charge – as described earlier, charge 34 is shown stored in floating gate 44 – instead, the entire stack 26

serves to "provide effective dielectric separation [insulation] between the control gate electrode 46 and the floating gate electrode 44" (col. 9, lines 15-17.)

Fig. 2 of Halliyal et al., then, shows a floating gate memory cell having a polysilicon floating gate 44, on which is formed a dielectric stack including a first oxide layer 28, a layer 30 including high-K dielectric material, and a second oxide layer 32. In the passage the Examiner cites in rejecting claim 26, Halliyal et al. say:

> Referring to FIG. 3, in the second step of the present invention ... a first oxide layer 28 is formed on an upper silicon surface 36 of the semiconductor substrate 16. In one embodiment, the upper silicon surface is the upper surface of a *polysilicon floating gate electrode*. In one embodiment, the semiconductor substrate 16 is a *single crystal silicon substrate*. The substrate 16 may comprise other elements of a semiconductor device. [Emphasis added.]

Referring to Fig. 3 of Halliyal et al., it will be seen that the bottom layer of the stack is denoted as "16 or 44," referring to either monocrystalline silicon substrate 16 of Fig. 1 or floating gate 44 of Fig. 2. There is no suggestion that the device be formed as a TFT in a polycrystalline substrate. There is certainly no disclosure of a SONOS device formed having a polysilicon channel. In the only embodiment in which the "modified ONO stack" of Halliyal et al. is formed on polysilicon, the polysilicon is a floating gate, and the device is not a SONOS device.

Claims 26, 36, 37, and 38 thus distinguish over the embodiment of Fig. 2 of Halliyal et al. for several reasons.

Claims 26, 36, 37, and 38 all include the limitation that the device *is a SONOS device*. The device of Fig. 2 of Halliyal et al. is a floating gate device, not a SONOS device. There is no disclosure in Halliyal et al. of a SONOS device with the claimed oxide-silicon nitride-oxide stack formed on polysilicon.

Additionally, claims 36 and 37 include the limitation that the first oxide layer is formed on a polysilicon *channel region*, not a polysilicon floating gate as in Fig. 2 of Halliyal et al.

Claims 26, 36, 37, and 38 all recite a contiguous stack of polysilicon, a first oxide layer, a silicon nitride layer on the first oxide layer, and a second oxide layer on the silicon nitride layer. Claims 36, 37, and 38 in fact specify that the first oxide layer is "in contact with" the polysilicon, the silicon nitride layer is "in contact with" the first oxide layer, and the second oxide layer is "in contact with" the silicon nitride layer, leaving no ambiguity that a contiguous stack is meant. For the reasons described in section A of this Argument, no embodiment of Halliyal et al. includes a first oxide layer, a silicon nitride layer, and second oxide layer in a contiguous stack.

Appellants have shown that claims 26 and 36-38 distinguish over Halliyal et al., and respectfully request that the 35 USC 102(e) rejections of these claims be withdrawn.

CONCLUSION

Accordingly, Appellants respectfully solicit the Honorable Board of Patent Appeals and Interferences to reverse the rejections of the pending claims and pass this application on to allowance.

Respectfully submitted,

November 22, 2005
Date

Pamela J. Squyres Reg. No. 52,246

Matrix Semiconductor, Inc.
3230 Scott Boulevard
Santa Clara, CA 95054
(408) 869-2921
(408) 869-8923 (fax)

VIII. CLAIMS APPENDIX

1-8. (Cancelled or withdrawn)

9. A method for making a SONOS device, comprising:

providing a channel region;

providing a first oxide layer on the channel region by an in-situ steam generation process;

providing a silicon nitride layer on the first oxide layer; and

providing a second oxide layer on the silicon nitride layer, wherein the device is a SONOS device.

10-11. (Cancelled)

12. The method of claim 9, wherein the in-situ steam generation process is performed at a temperature ranging from about 750 to about 1050 degrees Celsius.

13. The method of claim 9, wherein the in-situ steam generation process is performed at a pressure ranging from about 100 millitorr to about 760 torr.

14. The method of claim 9, wherein the in-situ steam generation process is performed for a time sufficient to deposit an oxide thickness of about 10 to about 200 angstroms.

15. The method of claim 9, further including annealing the oxide layer in a nitric oxide atmosphere.

16-23. (Cancelled or withdrawn)

24. A SONOS semiconductor device made by a method comprising:

providing a channel region;

providing a first oxide layer on the channel region by an in-situ steam generation process;

providing a silicon nitride layer on the first oxide layer; and

providing a second oxide layer on the silicon nitride layer wherein the device is a SONOS semiconductor device.

25. (Withdrawn)

26. An integrated circuit containing a SONOS semiconductor device made by a method comprising:

providing a polysilicon layer;

providing a first oxide layer on the polysilicon layer by an in-situ steam generation process;

providing a silicon nitride layer on the first oxide layer; and

providing a second oxide layer on the silicon nitride layer wherein the device is a SONOS semiconductor device.

27-35. (Cancelled or withdrawn)

36. A method for making a SONOS device, comprising:

providing a polysilicon channel region;

providing a first oxide layer in contact with the polysilicon channel region by an in-situ steam generation process;

providing a silicon nitride layer in contact with the first oxide layer; and

providing a second oxide layer in contact with the silicon nitride layer.

37. A SONOS semiconductor device made by a method comprising:

providing a polysilicon channel region;

providing a first oxide layer in contact with the polysilicon channel region by an in-situ steam generation process;

providing a silicon nitride layer in contact with the first oxide layer; and

providing a second oxide layer in contact with the silicon nitride layer.

38. An integrated circuit containing a SONOS semiconductor device made by a method comprising:

providing a polysilicon layer;

providing a first oxide layer in contact with the polysilicon layer by an in-situ steam generation process;

providing a silicon nitride layer in contact with the first oxide layer; and

providing a second oxide layer in contact with the silicon nitride layer, wherein the device is a SONOS semiconductor device.

39-42. (Cancelled or withdrawn)

IX. EVIDENCE APPENDIX

Exhibits A and B, following this sheet, are included as evidence.

Exhibit A

Design Considerations in Scaled SONOS Nonvolatile Memory Devices

Jiankang Bu and Marvin H. White
Sherman Fairchild Laboratory, 16A Memorial Dr. E., Lehigh University, Bethlehem, PA 18015
Phone: (610) 758-4421 Fax: (610) 758-6705 Email: jib2@lehigh.edu and mhw0@lehigh.edu

Abstract — Scaling the programming voltage, while still maintaining 10-year data retention time, has been always a big challenge for Poly-Oxide-Nitride-Oxide-Silicon (SONOS) researchers. We describe our progress in the design and scaling of SONOS nonvolatile memory devices. –9V +10V (1ms) programmable SONOS devices ensuring 10 years retention time after 10^7 Erase/Write cycles at 85°C have been developed successfully. Deuterium anneal, applied in SONOS device fabrication for the first time, improves the endurance characteristics better than traditional hydrogen or forming gas anneal. In this paper, we describe scaling considerations and process optimization along with experiments and characterization results.

TABLE OF CONTENTS

1. INTRODUCTION

Next generation high density electrically erasable programmable read-only memories (EEPROMs) require an endurance in excess of 10^6 erase/write cycles with 10-year data retention at 85°C and low programming voltages 5-10V [1] [2]. Two basic types of EEPROMs exist, namely, the floating gate device and the floating trap device, i.e. SONOS [3-4]. The floating gate device stores charge in the polysilicon as free carriers as a continuous spatial distribution in the conduction band, and the SONOS stores charge in spatially isolated deep level traps (Fig. 1).

The floating-gate memory has been running out of steam with respect to scaling cell-size and program/erase voltages. The relatively thick (7-12 nm) tunnel oxide in the floating-gate type memories provides good 10-year data retention; however, the high voltage requirement [5] has created a reliability issue, as it has exceeded the voltage limits of scaled CMOS devices. Dielectric hot carrier degradation, punch-through avalanche effects and high voltage junction breakdown [6-8] limit the lateral scaling to achieve high density. The concern over the loss of the entire memory charge through a single defect in the tunnel oxide limits vertical scaling and lower programming voltages [2], which increases support circuitry area and reduces the array efficiency.

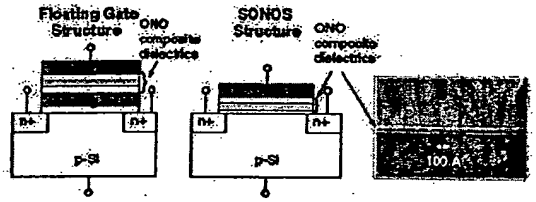

Fig. 1 Floating gate memory and floating trap (SONOS) with device cross-section.

The demand for low-power, low voltage electronics has accelerated the pace for NVSM circuit designers to consider SONOS for low voltage, high density EEPROM's. The motivation for the interest in SONOS lies in low programming voltages, endurance to extended erase/write cycling, resistance to radiation, and compatibility with high density scaled CMOS technology. A 3V, 1Mb, full-featured SONOS EEPROM has been manufactured using 0.8 μm CMOS technology [9]. Fujiwara et al. reported a 0.13 μm SONOS single transistor memory cell [10] with unselected word line bias for program-disturb improvement with subsequent scaling to 0.1 μm and beyond [11].

A radiation-hardened, SONOS based 4K gate field programmable gate array (FPGA) device has been described in 0.8 μm triple-level metal technology [12]. In this array SONOS transistors provide program connectivity and, for the first

time, offer the feature of reconfigurability in a FPGA device. SONOS NVSMs are capable of a small cell size ($6F^2$ where F = feature size) [13]. The ultra-thin tunnel oxide can conduct high current via direct tunneling with less charge trapping and a dramatic increase in charge-to-breakdown, Q_{BD}, with tunnel oxide thickness less than 3.2 nm – the mean free path of electrons in the oxide. Thus, we have the possibility of thin tunnel oxide SONOS devices for dynamic/quasi-nonvolatile memory applications, as discussed by Wann et al. [14] and King et al. [15].

A considerable effort has been devoted to scaling the programming voltages of SONOS devices with improved retention characteristics under extended erase/write cycling at elevated temperatures. Minami and Kamigaki reported a SONOS device with 10-year data retention after 10^7 erase/write cycles with programming voltage –11V +13V (1ms) [16]. Reisinger et al. proposed a p+ gate SONOS structure [17] to improve erase speed and data retention time. Libsch et al. [18], French and White [19], Yang and White [20] have all discussed a 5-8V EEPROM cell for high density NVSM.

Recently, we have explored the scaling of low voltage, long retention SONOS memory devices. SONOS devices fabricated at Lehigh University show a 0.5V detection window at 10-year data retention after 10^7 erase/write cycles at 85°C with programming voltage –9V +10V (1ms). We will describe scaling and process optimization in the Section 2. SONOS device fabrication and characterization results are described in Sections 3 and 4, respectively.

2. SCALING CONSIDERATIONS -- PROCESS OPTIMIZATION--

2.1 ONO Stack Scaling

Three approaches have been described in the literature to obtain good balance between speed, retention and endurance. One approach, taken by Roy and White [21], is to scale the nitride storage layer, but keep the blocking oxide thicker, which increase the memory window (will decrease for scaled nitride layer otherwise) and the amount of charge trapped at nitride/blocking oxide interface is increased too. Another approach, taken by Minami and Kamigaki [15], and Dellin et al. [22], uses a thin blocking oxide just thick enough to block the injection of charge from the gate, and scale the nitride layer at the same time. The other approach, investigated by Williams et al. [23] and Kapoor et al. [24], employed an oxynitride instead of the nitride as the storage medium, because the oxynitride film has a smaller trap density and hence a smaller Coulombic repulsion between the trapped charges. The tunnel oxide can be further scaled with or without a blocking oxide. In addition, Hu and White [25] have presented a buried channel device instead of a surface channel device to reduce back tunneling.

The work presented in this paper is based on the first approach, namely, incorporating the optimization of the tunnel oxide thickness [26]. For 8-10V program/erase voltages, a 10 nm effective gate dielectric thickness is preferred to guarantee an electric field for modified Fowler-Nordheim tunneling [27]. A 2.0 nm tunnel oxide and thicker blocking oxide (5.5 nm) are used for good retention and reliability considerations. The scaling of the nitride layer is based on the constant tunnel oxide electric field theory, which we will detail in Section 4 with a comparison of different design approaches.

2.2 Process Optimization

In our scaling, a trap-rich, silicon nitride (with a $SiCl_2H_2$: NH_3 ratio of 10:1) is necessary, as silicon nitride films deposited with high $SiCl_2H_2$: NH_3 gas flow ratios show high trap densities, which facilitate fast programming speed [28]. Yang et al. [29] conducted AFM studies on silicon nitride films, which were deposited at different temperatures. Their studies revealed 680°C as the optimum temperature for LPCVD nitride deposition for a minimum surface roughness with improved memory retention. Minami et al. demonstrated LPCVD formed blocking oxides improved data retention dramatically [15]. In addition, tunnel oxides grown at high temperature, exhibit improved performance and reliability [30]. Superior retention and endurance are obtained with the use of a triple-wall oxidation furnace rather than the conventional single-wall furnace [25].

We have performed high temperature (700°C 4 hours) deuterium anneals instead of hydrogen forming gas anneals after the contact windows are opened. Anneal temperatures comparable to or lower than the nitride deposition temperature provide less migration of the stored charge in the nitride [15]. Also, the interface states generation is reduced under extended program/erase cycling and retention reliability is improved as described in Section 4.

3. SONOS DEVICE FABRICATION

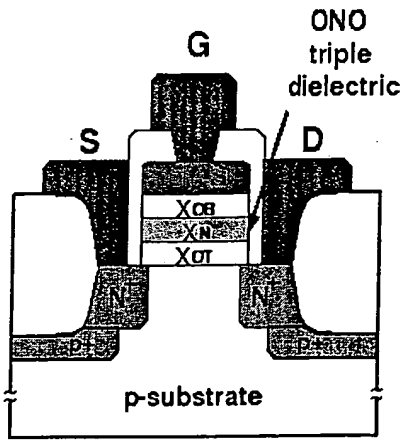

Fig. 2 Device structure of SONOS nonvolatile memory transistor with tunnel oxide 2.0 nm, nitride layer 4.5 nm, and blocking oxide 5.5 nm.

We have fabricated SONOS devices with N-well CMOS technology and LOCOS isolation. The processing sequence is identical to conventional CMOS technology except for the formation of the ONO dielectric stack. The key process steps are as follows: A 2.0 nm thick tunnel oxide is grown at 800°C for 40 min. with argon-diluted oxygen (1% O_2 in Ar) in a custom-designed triple wall oxidation furnace followed by 30 min. argon anneal to relieve the stress caused by high temperature oxidation. Next, a 4.5 nm silicon nitride is deposited in a LPCVD reactor for 15 min. at 680°C with gas flow ratio of $SiCl_2H_2$: NH_3 = 100:10 (sccm). A 5.5 nm LPCVD blocking oxide is deposited with $SiCl_2H_2$: N_2O = 10:100 (sccm) at 725°C followed by a steam densification at 900°C for 30 min. After the ONO triple dielectric film is formed, a layer of polysilicon is deposited and doped in a $POCl_3$ process. Next, the gate is patterned and the contact windows are opened. A 4 hour 10% D_2/N_2 anneal at 700°C is performed to lower the interface state density. This is followed by an aluminum deposition for contact metallization with a post-metal-anneal (PMA) at 400°C for 30 min. in 10% D_2/N_2. For comparison purposes, another group of wafers annealed with 10% H_2/N_2 are fabricated at the same time. Fig. 2 shows the device structure.

4. MEASUREMENT RESULTS AND DISCUSSION

In this section, we present erase/write, retention and endurance electrical characteristics of scaled SONOS devices. The threshold voltage shifts are measured 1 μs after an erase (write) pulse that follows a 10 s low voltage reset pulse of reverse polarity. All measurements are made at 85°C unless specified. We compare the effects of high temperature deuterium and hydrogen anneals.

Fig. 3 shows the erase/write characteristics. The SONOS device can be operated with a 1 ms –9V/+10V pulse. In the +10V write or program operation, the initial electric field across the tunnel oxide is 11.8 MV/cm with 9.8 MV/cm for the –9V erase operation. In previous MONOS/ SONOS scaling scenarios the electric field across the tunnel oxide or nitride has been maintained nearly constant while the triple dielectric dimensions are scaled [31-32]. Using the constant tunnel oxide electric field theory as the criteria, we compared devices scaled along different approaches in Fig. 4. For the device with 1.8 nm tunnel oxide reported by Minami et al. [16], the initial electric field at 13V is approximately 10MV/cm, assuming zero stored nitride charge.

If we scale the nitride from 13 nm to 4.5 nm and thicken the tunnel and blocking oxides to maintain the same initial electric field, then we have a 10 nm effective gate dielectric thickness with a programming voltage decreased to 9V. However, a smaller memory window and earlier saturation are observed with our scaled nitride device. A thicker tunnel oxide and blocking oxide compensates for the barrier lowering effect due to Coulombic repulsion in the scaled nitride layer (associated with degraded retention) and offers highly-reliable retention characteristics. French et al. [27] noticed scaling the blocking oxide does not improve the erase/write speed of the device. Fig. 5 illustrates the retention and endurance characteristics of our device. 10-year data retention with 0.5V memory window after 10^7 erase/write cycles at 85°C is ensured.

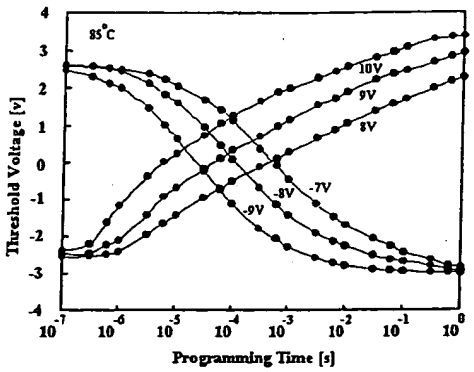

Fig. 3 Erase/write characteristics for scaled SONOS device with tunnel oxide 2.0nm, nitride 4.5nm, blocking oxide 5.5nm.

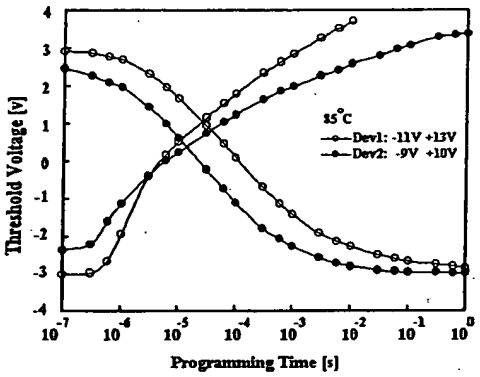

Fig. 4 Comparison of SONOS/MONOS devices with different design approaches. Dev1: tunnel oxide 1.8nm, nitride 13nm, blocking oxide 3nm. Dev2: tunnel oxide 2.0nm, nitride 4.5nm, blocking oxide 5.5nm.

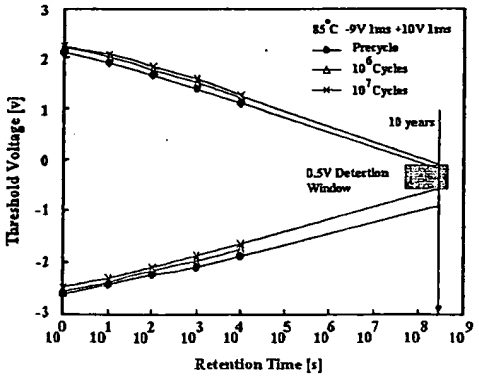

Fig. 5 Retention characteristics after erase/write cycles for SONOS device with tunnel oxide 2.0nm, nitride 4.5nm, blocking oxide 5.5nm.

The deterioration of $Si-SiO_2$ interface is of major concern in NVSM devices because of the high electric fields across the insulators and the continual passage of charge across the tunnel oxide region. This deterioration manifests itself as a buildup of "interface traps", which are defect centers located at the $Si-SiO_2$ interface. Their build-up, along with traps exist between $SiO_2-Si_3N_4$ layer, is detrimental to both SONOS and floating-gate NVSM operation because they (1) provide an additional shift in the device threshold voltage and (2) degrade long-term retention by increasing the so-called back-tunneling current [33]. Maes et al. have employed high temperature hydrogen anneals to reduce interface trap density and improve data retention time [34].

The channel hot carrier lifetime of MOSFETs, annealed in a deuterium ambient instead of the traditional hydrogen or forming gas ambient, have increased by an order of magnitude [35]. In an extension of these studies, we have examined high temperature deuterium anneals in the fabrication of SONOS devices. Fig. 6 compares the interface trap densities (D_{it}) of SONOS devices annealed in deuterium and hydrogen environments. The initial D_{it} is nearly the same for both devices. However, under extensive erase/write cycling, more interface traps are created for hydrogen annealed devices than with deuterium annealed devices.

The retention characteristics of hydrogen annealed SONOS devices are shown in Fig. 7. In contrast with Fig. 5, deuterium annealed SONOS devices have nearly an order of magnitude longer retention time after 10^7 erase/write cycles at 85°C than hydrogen annealed devices for the same detection window. Studies have been conducted to investigate this isotopic interfacial hardening effect [36]. These studies suggest the improved robustness of interface states to dissociation is associated with the difference in vibration mode frequencies of the Si-H and Si-D configurations. The vibration frequency of the bending mode for Si-D bonds is around 460 cm^{-1}, which is very close to the frequency of one of the bulk silicon phonon modes (463 cm^{-1}). Coupling of these modes can provide an energy relaxation channel and make the dissociation of Si-D bonds more difficult than the dissociation of Si-H bonds.

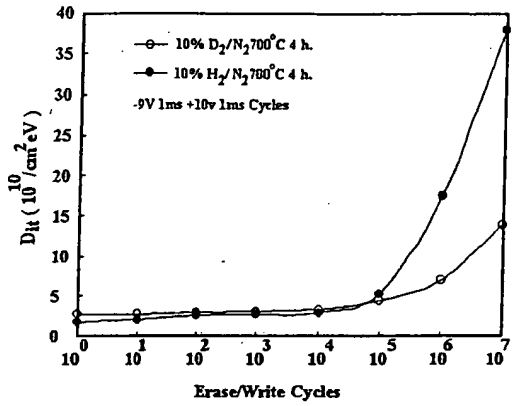

Fig. 6 Dit variation of high temperature deuterium annealed and hydrogen annealed devices.

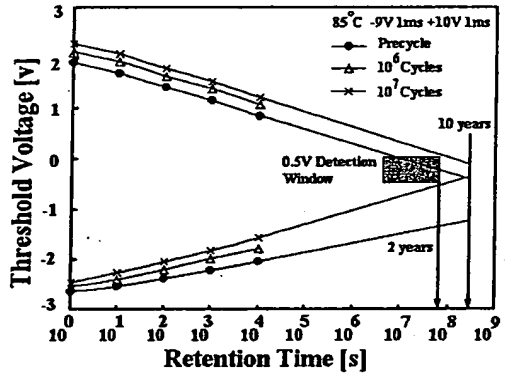

Fig. 7 Retention characteristics of a hydrogen-annealed SONOS device. Compared with deuterium-annealed SONOS in Fig. 5, retention time is nearly one order of magnitude shorter for the same detection window.

5. CONCLUSIONS

SONOS nonvolatile memory devices exhibit a 0.5V detection window with 10-year data retention after 10^7 erase/write cycles at 85°C, with 1 ms +10V/–9V program/erase voltages. Deuterium annealing offers improved endurance characteristics over traditional hydrogen forming gas anneals. These SONOS devices are promising candidates for low voltage, radiation-hardened, high-density EEPROM's applications.

6. ACKNOWLEDGMENTS

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8. BIOGRAPHIES

Jiankang Bu was born in Hebei Province, China on February 4, 1972. He received his B.S. degree (1994) and M.S. degree (1997) in Electrical Engineering from Nankai University, China. He joined the Electrical Engineering Dept. at Lehigh University in the Fall 1997 as a research assistant. He is currently working on his Ph.D degree in Electrical Engineering on measurement circuit design, device characterization and fabrication of scaled SONOS nonvolatile memories. He is a member of the IEEE Electron Devices Society (EDS) and the Sigma Xi research honorary.

Marvin H. White was born in the Bronx, New York on September 6, 1937. He received an A.S. degree in Engineering from the Henry Ford Community College (1957) a B.S.E. degree in Physics and Math (1960), M.S. degree in Physics (1961) from the University of Michigan and a Ph.D. degree in Electrical Engineering (1969) from the Ohio State University. In 1961 he joined the Westinghouse Solid-State Laboratory in Baltimore, MD. where he worked on advanced military and NASA imaging systems. From 1961 - 1981 he worked at Westinghouse as an Advisory Engineer in the design of low-power, custom integrated circuits with technologies of CMOS, Bipolar, MNOS and CCDs. During this period he was an adjunct Professor at the Electrical Engineering Depart-ment of the University of Maryland and a visiting Fulbright Professor at the Catholique Universite' de Louvain in Louvain-la-Neuve, Belgium.

In 1981, he became the Sherman Fairchild Professor in Solid-State Studies and Electrical Engineering at Lehigh University. At Lehigh he has developed a graduate program in microelectronics with research on SONOS nonvolatile memory devices, CMOS device modeling, studies of the Si-SiO_2 interface, SiC devices, and custom integrated circuits and sensors. He has graduated 23 Ph.D. students in microelectronics. He has served as a Visiting Researcher at the Naval Research Laboratories (1987) and a Program Director in Solid- State and Microstructures at the National Science Foundation (1995-96). In 1997 he received the Eleanor and Joseph Libsch Research Award at Lehigh University. He is currently the Director of the Sherman Fairchild Center for Solid-State Studies.

Prof. White is an IEEE Fellow (1974) and the recipient of the J. J. Ebers Award (1997) and the Masaru Ibuka IEEE Consumer Electronics Award (2000). In 1982 he was the IEEE Electron Devices Society (EDS) National Lecturer and is presently a Distinguished EDS Lecturer. He has served on IEEE/EDS committees, in particular, membership, and education. He is a member of Eta Kappa Nu and Sigma Xi.

Exhibit B

FEATURING

A Device that Has Traveled in Outer Space

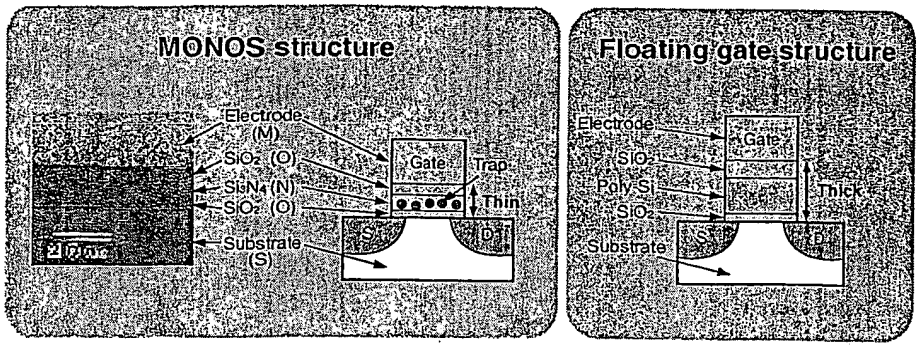
Low-Cost Embedded Nonvolatile Memory Device Technology: MONOS

- **High reliability**
  – Charge storage in a nitride film –
- **Narrow distribution of threshold voltages obviates the need for a "verify" operation to match distribution widths narrowly**
  – Makes circuit design easier –
- **Simple device structure makes chips easier to manufacture**
  – Expected to be usable through the 0.1 μm generation –
- **Low-cost embedded nonvolatile memory technology**
  – Low-voltage write and erase operations achieved by the use of hot carrier injection–

While MONOS (metal–oxide-nitride-oxide-semiconductor) is not a new nonvolatile memory technology, it has not received much attention until recently. The floating gate technology has remained as the mainstream nonvolatile memory technology, mostly due to the MONOS data retention characteristics being inferior. However, MONOS' reputation has begun to change over in recent years.

Figure 1 compares the MONOS and floating gate device structures. As can be seen in figure 1, the MONOS name comes directly from the structure of the device. (In the US, silicon is used instead of metal, and it is called SONOS.) In MONOS, charge is stored in traps in the nitride layer, which is an insulator sandwiched between oxide layers, and this stored charge is used to record data. In the US, MONOS is used in satellites and spacecraft that wander for long periods between the planets. So why is it that MONOS, which is thought to have poor data retention characteristics, is used in the harsh environment of outer space, where they are constantly bombarded by high-energy particles? The reason lies in the structure and operating principles of the MONOS device. MONOS devices are actual highly stable and reliable devices.

Recently, the idea of storing 2 bits in a single memory transistor cell by using the features associated with storing charge on in the insulation layer in the MONOS device has been proposed. This makes it possible for MONOS to be the highest density nonvolatile memory technology, and has resulted in increasing interest in this technology. Another point is that the limits of the floating gate nonvolatile memory technology are now in sight, and MONOS is seen as having the potential to be the next generation nonvolatile memory technology. Sony's researchers already see how MONOS can be adapted for use through the 0.1 μm feature size generation. Furthermore, Sony is now developing MONOS as a key technology for product differentiation in Sony's system-on-chip (SoC) business.



■ Figure 1 MONOS and Floating Gate Structures Comparison

MONOS Device Structure and Operating Principles

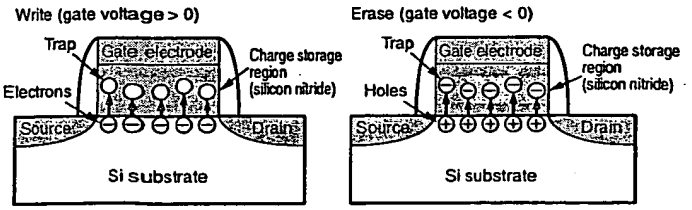
As shown in figure 1, the MONOS structure consists of ONO film layers (oxide-nitride-oxide) between the substrate and the gate. While the nitride film in the center of the ONO film layers is an insulator, there are large numbers of traps located in that layer and it can capture and store charge. This layer can be made to function as a charge storing means by injecting and rejecting charge from these traps.

There are two techniques for injecting and rejecting charge. One is a write and erase method in which electrons are injected or rejected with tunnel current technique over the whole area under the gate electrode as shown in figure 2. The other method uses hot carriers as shown in figure 3. The tunnel current technique achieves a larger number of write/erase cycles and assures high reliability. In contrast, the hot carrier method allows lower write and erase operating voltages to be used and achieves higher speeds. Lowering the operating voltage also leads to reduced manufacturing costs, and is effective for one-time programming (OTP) and multi-time programming (MTP) products. Recently, the idea of MONOS devices that store 2 bits in a single memory transistor cell using this principle has proposed. These are called NROM devices.

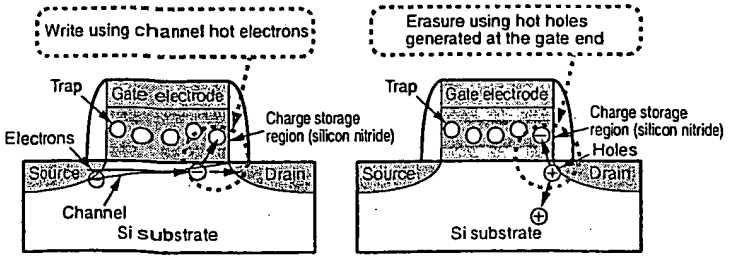
High Reliability

MONOS' main advantage lies in its stability and durability. As shown in figure 4, there is almost little charge leakage in MONOS devices even if there are defects in the extremely thin oxide film between the nitride layer that stores the charge and the substrate. This is because charge is stored in an insulating film layer. In contrast, in the floating gate type device, all stored charge is lost if a defect is created at even one location. This is like the shipbuilding technique in which large numbers of isolated chambers are used. If a defect is opened in one, the area that is flooded is limited to that chamber. That is, even if a defect is created between the substrate and the layer (nitride film) that stores the charge, it is impossible for all the charge stored in the insulating film to escape through that defect. In contrast, conventional floating gate ships (devices) would flood and sink immediately if even one defect appeared. This is because the floating gate, which stores the charge, is itself a conductor. This MONOS durability is the reason MONOS is used in outer space, where devices are constantly bombarded by high-energy particles.

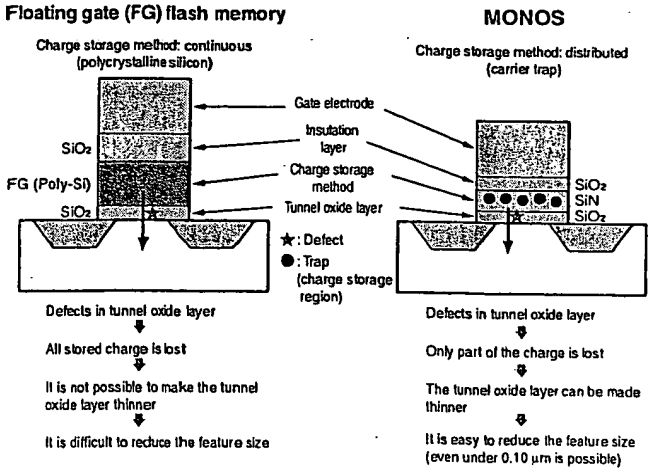
MONOS has another advantage. That advantage is that it leaks. It cannot be denied that this is the reason that MONOS is not widely used. However, as our study of the MONOS structure has progressed, and we have had more experience using MONOS, we have come to realize the following. There is no sample-to-sample variation in the amount of leakage in MONOS devices. That is, all boats (devices) leak water at the same rate. This means that it is possible to predict when to get off the boat in safety. That is, these boats are actually much safer than boats that appear solid but may actually rupture and sink at any time.



■ Figure 2 MONOS Write and Erase Operations Using F-N Tunnel Current Injection Technique Conceptual Overview



■ Figure 3 MONOS Write and Erase Operations Using Hot Carriers Injection Technique Conceptual Overview



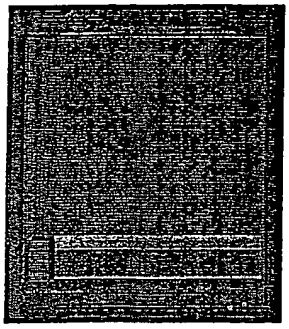
■ Figure 4 MONOS Features: Charge Does not Escape even with Defects in the Oxide Layer

Narrow Threshold Voltage Distribution Obviates the Need for Operations to Narrow the Distribution

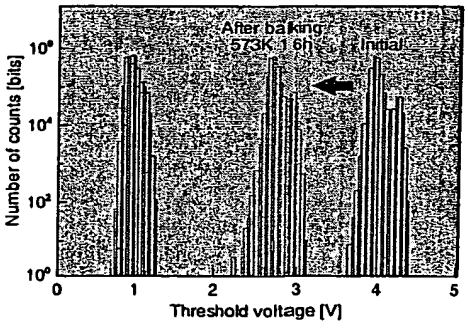
Sony has taken the lead in this area by creating the 4 Mbit MONOS test memory chip shown in figure 5. (This device was announced at the 2001 IEDM conference.) Figure 6 shows the accelerated test results for the written threshold voltage distribution retention characteristics. Although the threshold voltage falls, the distribution does not break. Furthermore, as shown in table 1, the width of the distribution itself is narrower, being only 1/3 that of the conventional floating gate device, and thus is extremely well matched. Also, the threshold voltage distribution does not break after repeated write and erase cycles. Figure 7(a) shows the change in the width of the distribution with writing, and figure 7(b) shows that change with erasure. As you can see, the width of the distribution does not change with these processes. Even with repeated write and erase cycles, the distribution remains narrow. (See figure 8.) This is one of MONOS' superior characteristics, and is a significant advantage when designing memory circuits. In the conventional floating gate device, the threshold voltage distribution must be narrowed with an operation called "verify" during write and erase. This is a difficult circuit operation and complicates circuit design. The MONOS structure may be able to obviate the need for this "verify" operation.

Device with a Simple Ease to Fabricate Structure

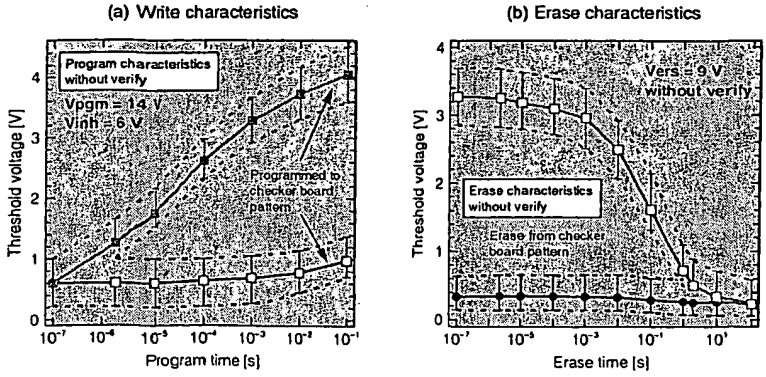
Another significant feature of the MONOS structure is the simplicity of that structure. Figure 9 shows the cross section of a MONOS device imaged with a transmission electron microscope (TEM). At first look, it appears to be identical to an ordinary MOS transistor. Sony already sees the way to use this structure in 0.1 μm generation devices. The simplicity of this structure is also extremely important for embedding these devices in larger chips. This is because the simpler the structure the fewer the additional fabrication steps required for embedding. If only MONOS transistors are added, only 2 or 3 mask steps need to be added. Normally, embedding other types of flash memory requires an additional 6 or 7 masks. This is because these other devices require that the high-voltage transistors that handle the high voltages required for write and erase operations must be created separately.



■ Figure 5 4 Mbit MONOS Test Chip



■ Figure 6 4 Mbit MONOS Test Chip Memory Retention Characteristics



■ Figure 7 Write and Erase Characteristics of MONOS Threshold Voltage Distribution

■ Table 1 MONOS and Floating Gate Threshold Voltage Distributions Comparison

	MONOS	Floating gate devices		
	This product	ref.1	ref.2	ref.3
Write state	0.057		0.165	
Erase state	0.058	0.15		0.15

Standard deviation (V)

Standard deviation in MONOS is about 1/3

[1] K.Yoshikawa, et al., IEDM92, p.595 (1992).
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[3] P.L.Rolandi, et al., NVSMW 2000, p.75 (2000).

Low-Cost Embedded Nonvolatile Memory Technology

If nonvolatile memory could be embedded with only the addition of 2 or 3 masks, that is, with only a cost increase of about 10% over that of the original chip, we could expect a large demand for OTP and MTP applications. Another way of looking at this would be that low-cost embedded nonvolatile memory technology would function as a product differentiation technology. Specific examples that would be possible include inclusion of embedded nonvolatile memory in the camera processor IC that forms, along with the CMOS image sensor, a camera module, in a GPS module that fits in a Memory Stick slot, or in a camera module interface chip. (See figure 10.)

Other applications where this would be useful include the programmable impedance matching circuit used in high-precision D/A converters and high-precision power supplies and the recording of data used for chip authentication.

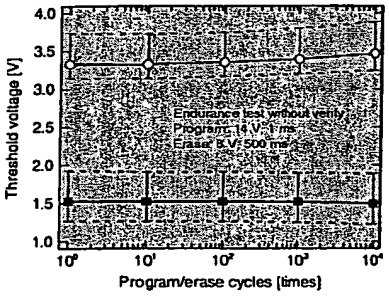
Sony is now studying the possibility of reducing the MONOS write and erase voltages to realize low-cost embedded nonvolatile memory technology using only 2 or 3 additional masks. Sony is attempting to reduce the voltages required by switching from the use of F-N tunnel current, which requires 12 to 14 V for write and erase, to a technique that uses hot carriers. Figure 11(a) shows the write characteristics when channel hot electrons are used, and figure 11(b) shows the erase characteristics using hot hole injection. With absolute voltages around 5 to 6 V, these techniques can achieve fully adequate write and erase operations.

Future Developments

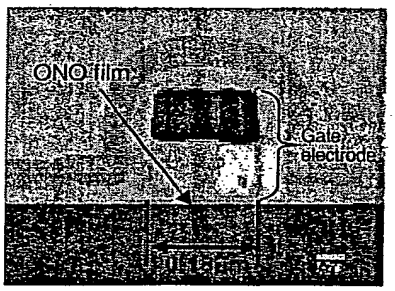
Sony is making progress on embedding MONOS nonvolatile memory in a 0.18 µm CMOS process. We are working on creating new applications and expect to release products using this technology during 2003.

This one process is not the only process that requires embedded nonvolatile memory. To take maximum advantage of this newly-developed technology, Sony plans to apply it in as many processes as possible. We think that MONOS' stability and durability will make this easy.

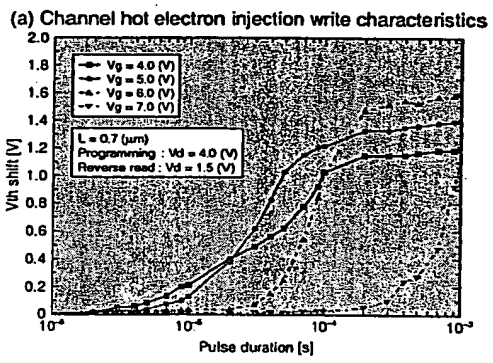
Keep your eye on Sony's low-cost nonvolatile memory technology.



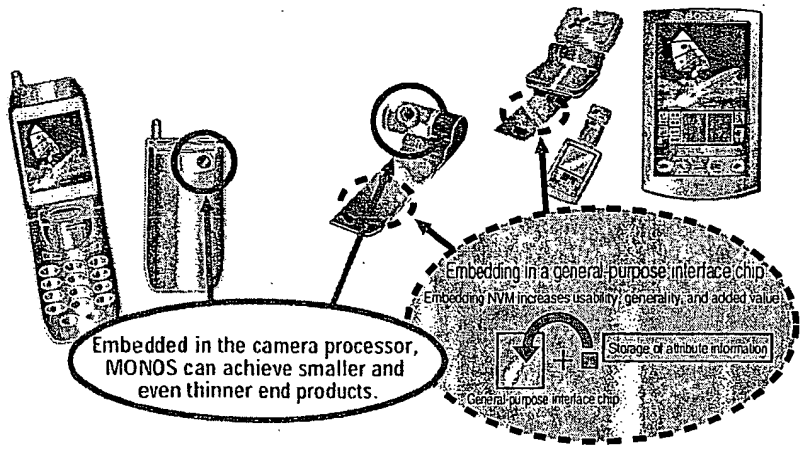
■ Figure 8 4 Mbit MONOS Test Chip Endurance Characteristics



■ Figure 9 TEM Photograph for MONOS Memory Transistor



■ Figure 11 Characteristics of the Embedded Low-Voltage MONOS Memory Cell



■ Figure 10 Embedded MONOS Applications

X. RELATED PROCEEDINGS APPENDIX

None.

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ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
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  - ☐ Affidavits/declaration(s)
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